HTG24064-05N-24H08-V01

产品名称（Product name） : 黑白点阵 COG

型　　号（Model） : HTG24064-05N-24H08-V01

编　　号（EDC number） :

日　　期（Date） : 2023-04-12

编码：QR-R-011　A/0　　序号：

深圳市鑫洪泰电子科技有限公司 Shenzhen Hot Display Technology Co.,Ltd		
编制 Prepared by	审核 Checked by	核准 Approved by

Rev.	Descriptions	Date
01	Prelimiay Release	2023-04-12
02		

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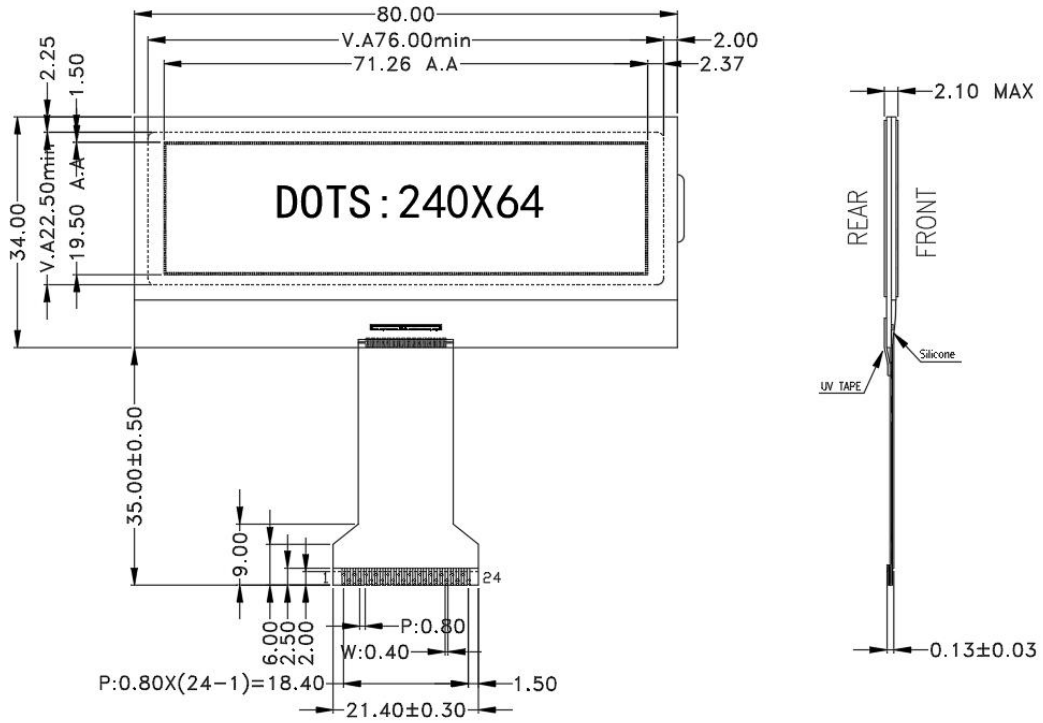
1.1 Display Specifications

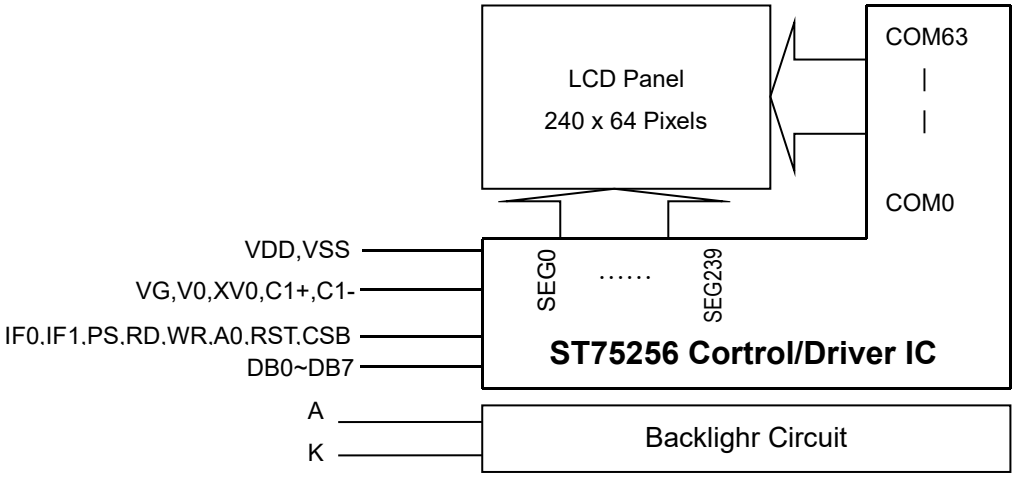
1>LCD Display Mode : STN-YG, Positive, Transmissive
2>Viewing Angle : 6H
3>Driving Method : 1/64 Duty, 1/9 Bias
4>Backlight :

1.2 Mechanical Specifications

1>Outline Dimension : 80.0x34.0 x 2.1mm (See attached Outline Drawing for Details)



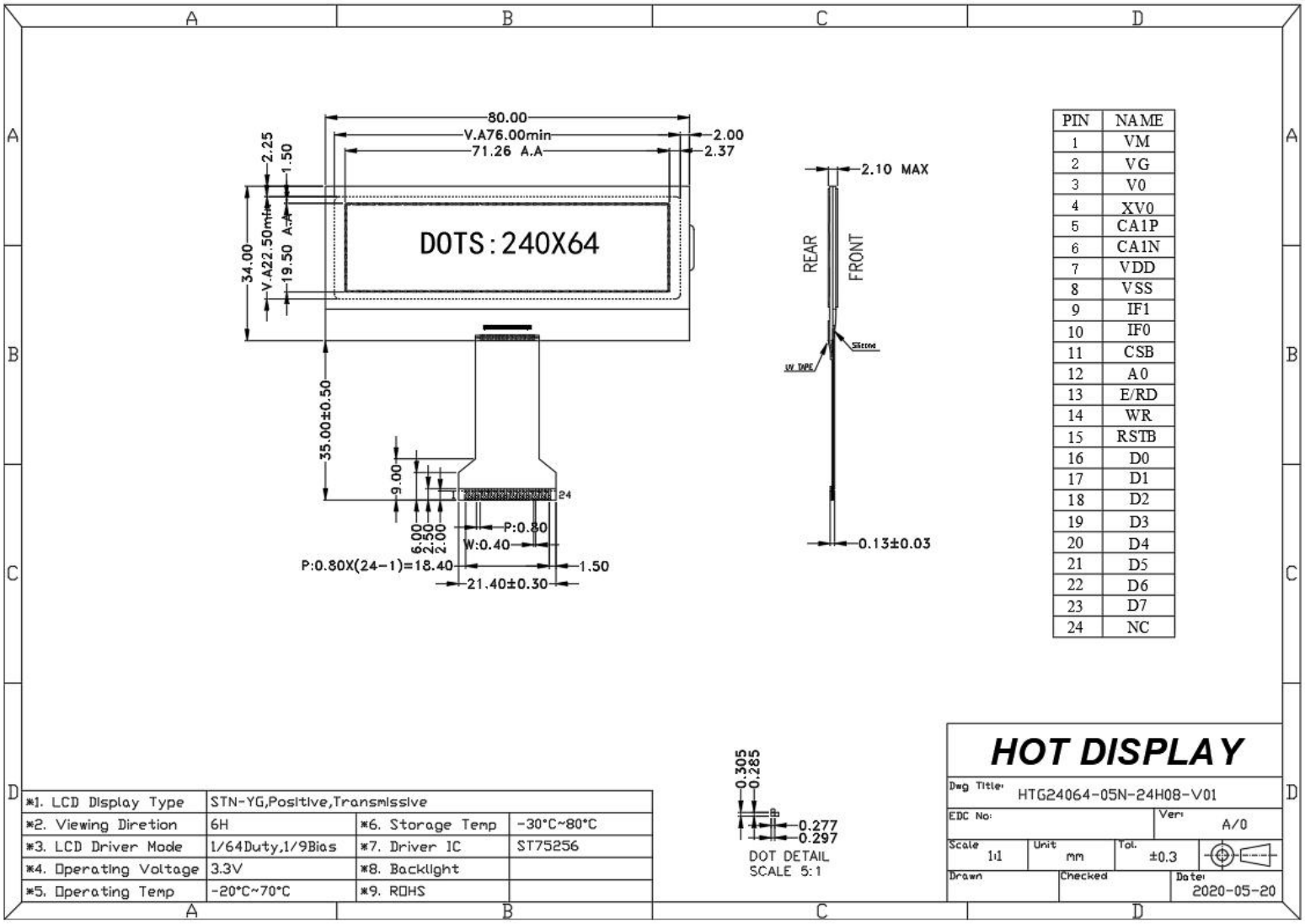
1.3 Circuit Diagram



1.4 Terminal Function

Pin No.	Pin Name	Function
1	VM	VM is the I/O pin of LCD bias supply voltage
2	VG	DC/DC voltage converter Connect a capacitor between VG and VSS.
3	V0	DC/DC voltage converter Connect a capacitor between V0 and XV0.
4	XV0	DC/DC voltage converter Connect a capacitor between XV0 and V0.
5	CA1P	DC/DC voltage converter. Connect a capacitor between CA1P and CA1N.
6	CA1N	DC/DC voltage converter. Connect a capacitor between CA1N and CA1P.
7	VDD	Positive power supply,3.3V
8	VSS	Negative power supply,0V
9	IF1	These pins select interface operation mode
10	IF0	These pins select interface operation mode
11	CSB	This is the chip select signal.
12	A0	Register select input pin A0 = “H” : DB0 to DB7 are display data A0 = “L” : DB0 to DB7 are control data
13	RD	Read (/RD) control signal input.
14	WR	Write (/WR) control signal input.
15	RSTB	Rester Pin(L->H)
16-23	D0~D7	8Bit-Data Bus
24	NC	NC

1.5 Product Outline



PIN	NAME
1	VM
2	VG
3	V0
4	XV0
5	CA1P
6	CA1N
7	VDD
8	VSS
9	IF1
10	IF0
11	CSB
12	A0
13	E/RD
14	WR
15	RSTB
16	D0
17	D1
18	D2
19	D3
20	D4
21	D5
22	D6
23	D7
24	NC

*1. LCD Display Type	STN-YG,Positive,Transmissive		
*2. Viewing Direction	6H	*6. Storage Temp	-30°C~80°C
*3. LCD Driver Mode	1/64Duty,1/9Bias	*7. Driver IC	ST75256
*4. Operating Voltage	3.3V	*8. Backlight	
*5. Operating Temp	-20°C~70°C	*9. ROHS	

HOT DISPLAY

Dwg Title: HTG24064-05N-24H08-V01
EDC No: Ver: A/0
Scale 1:1 Unit mm Tol. ±0.3
Drawn Checked Date: 2020-05-20

2. Absolute Maximum Ratings

Items	Symbol	MIN.	MAX.	Unit	Condition
Supply Voltage	VDD	-0.3	+3.6	V	Vss = 0V
Input Voltage	VIN	-0.3	VDD+0.3	V	Vss = 0V
Operating Temperature	TOP	-20	+70	℃	No Condensation
Storage Temperature	Tst	-30	+80	℃	No Condensation

3. Electrical Characteristics

3.1 DC Characteristics

Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Operating Voltage	VDD	3.0	3.3	3.6	V	VDD
Input High Voltage	VIH	0.8 x VDD	-	VDD	V	CSB,/RST,A0,WR, RD,D0~D7,
Input Low Voltage	VIL	Vss	-	0.2 x VDD	V	
Output High Voltage	VOH	0.8 x VDD	-	VDD	V	D0~D7
Output Low Voltage	VOL	Vss	-	0.2 x VDD	V	D0~D7
Input Leakage Current	ILI	-1.0	-	1.0	μA	VDD
Output Leakage Current	ILo	-3.0	-	3.0	μA	VDD

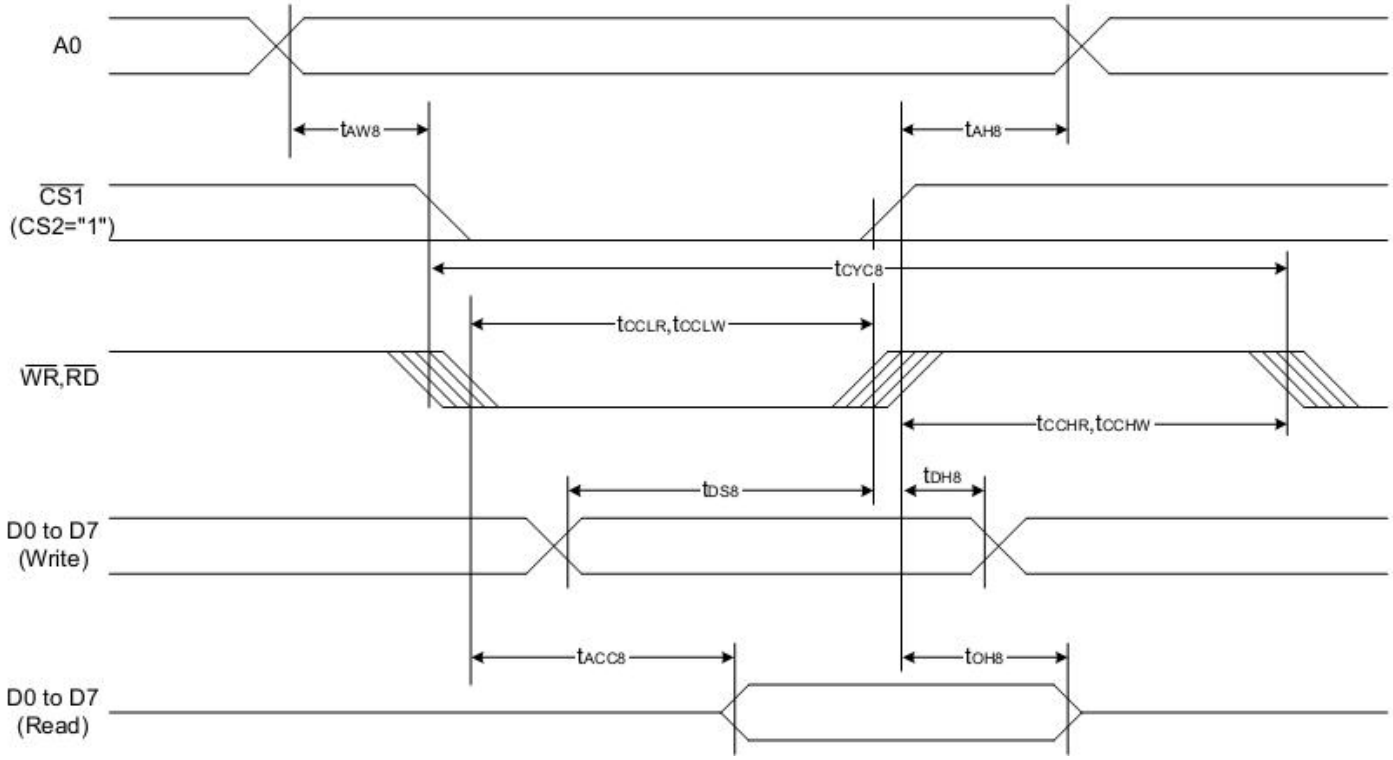
3.2 LED Backlight Circuit

Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
Forword Voltage	Vf BLA	-	-	-	V	VDD
Forword Current	If BLA	-	-	-	mA	VDD

3.3 AC Characteristics

3.3.1 8080 Mode System Bus Timing



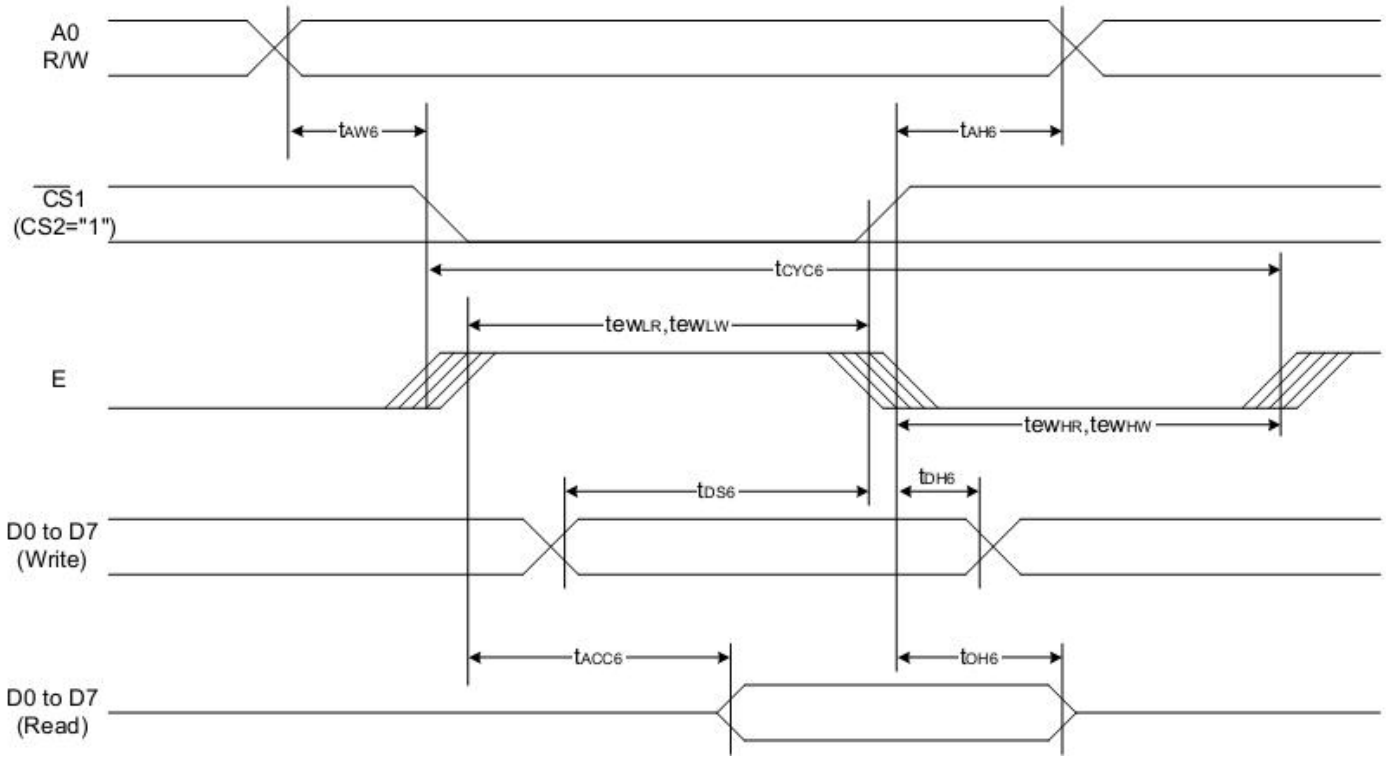
Vss = 0V,Top = 25℃

Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
System cycle time	Tcyc8	160	-	-	ns	-
Address setup time(A0)	Taw8	20	-	-	ns	-
Address hold time(A0)	Tah8	0	-	-	ns	-
Control Low Pulse wide(/RD)	tcclr	180	-	-	ns	-
Control Low Pulse wide(/WR)	tcclw	70	-	-	ns	-
Control High Pulse wide(/RD)	tcchr	180	-	-	ns	-
Control High Pulse wide(/WR)	tcchw	70	-	-	ns	-
Data steup time	Tds8	15	-	-	ns	-
Data hold time	Tdh8	0	-	-	ns	-
/RD access time(*a)	Tacc8	-	-	-	ns	-
Output disable time(*a)	Tch8	15	-	-	ns	-

Note:

***a. all timing is using 20％ and 80％ of VDD as the reference.**

3.3.2 6800 Mode System Bus Timing



Vss = 0V,Top = 25℃

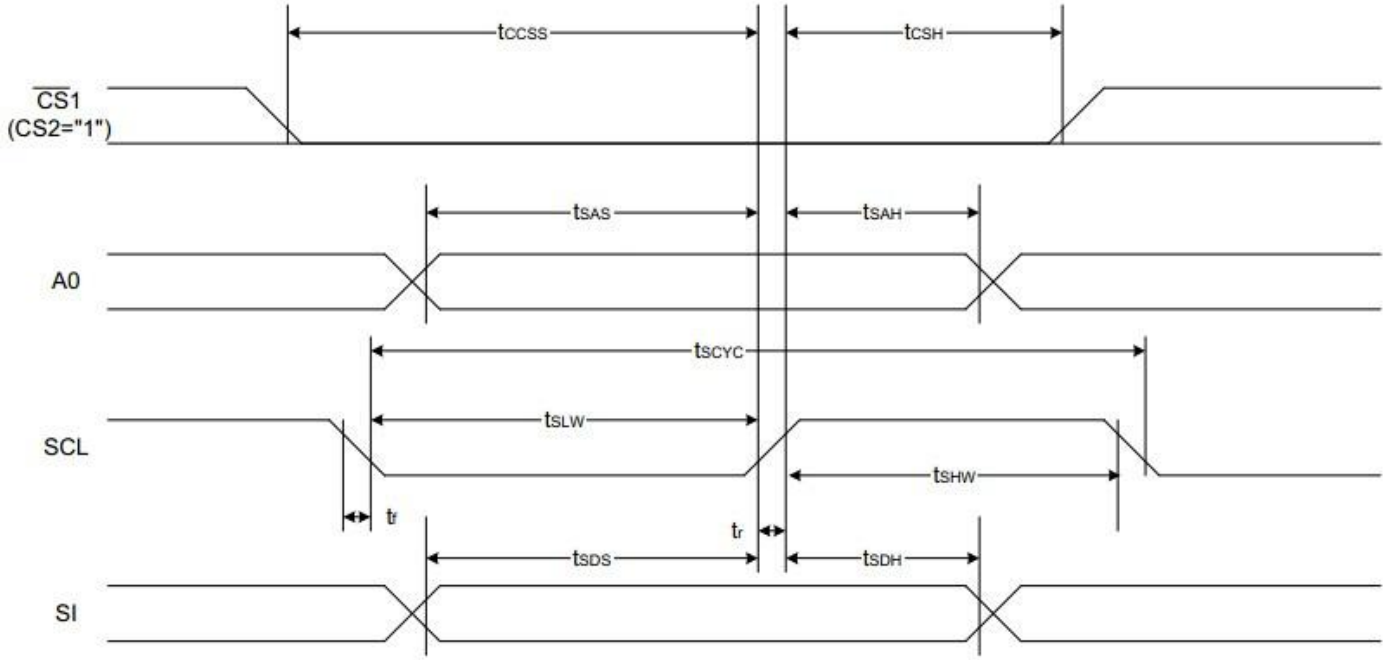
Items	Symbol	MIN.	TYP.	MAX.	Unit	Condition
System cycle time	Tcyc6	160	-	-	ns	-
Address setup time(A0)	Taw6	20	-	-	ns	-
Address hold time(A0)	Tah6	0	-	-	ns	-
Control Low Pulse wide(/RD)	tcclr	180	-	-	ns	-
Control Low Pulse wide(/WR)	tcclw	70	-	-	ns	-
Control High Pulse wide(/RD)	tcchr	180	-	-	ns	-
Control High Pulse wide(/WR)	tcchw	70	-	-	ns	-
Data steup time	Tds6	15	-	-	ns	-
Data hold time	Tdh6	0	-	-	ns	-
/RD access time(*a)	Tacc6	-	-	200	ns	-
Output disable time(*a)	Tch6	15	-	150	ns	-

Note:

***a. all timing is using 20％ and 80％ of VDD as the reference.**

***b. CL = 100pF**

3.3.3 4-line SPI Mode



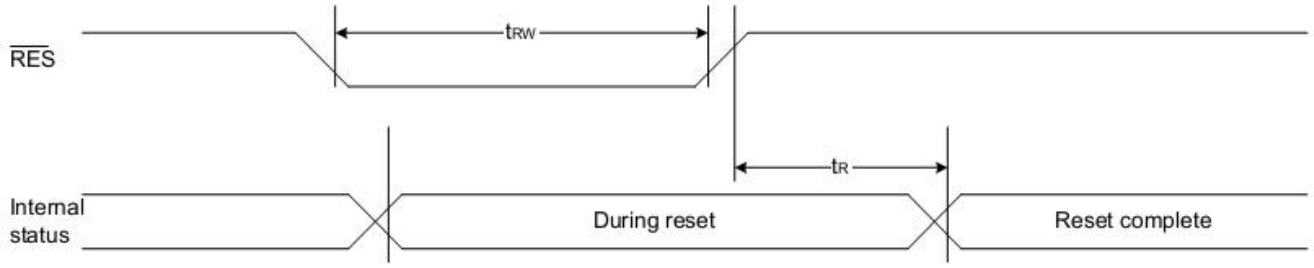
(V_{DD} = 3.3V, Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	Tscyc		50	—	ns
SCL "H" pulse width		Tshw		25	—	
SCL "L" pulse width		TSLW		25	—	
Address setup time	A0	TSAS		20	—	
Address hold time		Tsah		10	—	
Data setup time	SI	Tsds		20	—	
Data hold time		TSDH		10	—	
CS-SCL time	CS	Tcss		20	—	
CS-SCL time		Tcsh		40	—	

(V_{DD} = 1.8V, Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating		Units
				Min.	Max.	
4-line SPI Clock Period	SCL	TSCYC		200	—	ns
SCL "H" pulse width		TSHW		80	—	
SCL "L" pulse width		TSLW		80	—	
Address setup time	A0	TSAS		60	—	
Address hold time		TSAH		30	—	
Data setup time	SI	TSDS		60	—	
Data hold time		TSDH		30	—	
CS-SCL time	CS	TCSS		40	—	
CS-SCL time		TCSH		100	—	

3.4 Reset Timing



(VDD = 3.3V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	1.0	us
Reset "L" pulse width	/RES	tRW		1.0	—	—	us

Table 37

(VDD = 2.7V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	2.0	us
Reset "L" pulse width	/RES	tRW		2.0	—	—	us

Table 38

(VDD = 1.8V,Ta = –30 to 85°C)

Item	Signal	Symbol	Condition	Rating			Units
				Min.	Typ.	Max.	
Reset time		tR		—	—	3.0	us
Reset "L" pulse width	/RES	tRW		3.0	—	—	us

Note:

***a. all timing is using 20％ and 80％ of VDD as the reference.**

4. Function specifications

4.1 The Parallel Interface

Common	6800-series		8080-series		Description
A0	E (ERD)	R/W (RWR)	/RD (ERD)	/WR (RWR)	
H	H	H	L	H	Display data read out
H	H	L	H	L	Display data write
L	H	H	L	H	Internal status read
L	H	L	H	L	Writes to internal register (instruction)

Table 1 Parallel/Serial Interface Mode

Type	IF2	IF1	IF0	Interface mode
Serial	L	L	L	4-line serial interface
	L	L	H	I^2C serial interface
	H	L	L	9 bit 3-line serial interface
Parallel	L	H	L	8bit 6800-series MPU mode
	L	H	H	8bit 8080-series MPU mode

4.2 External Component of Power Circuit

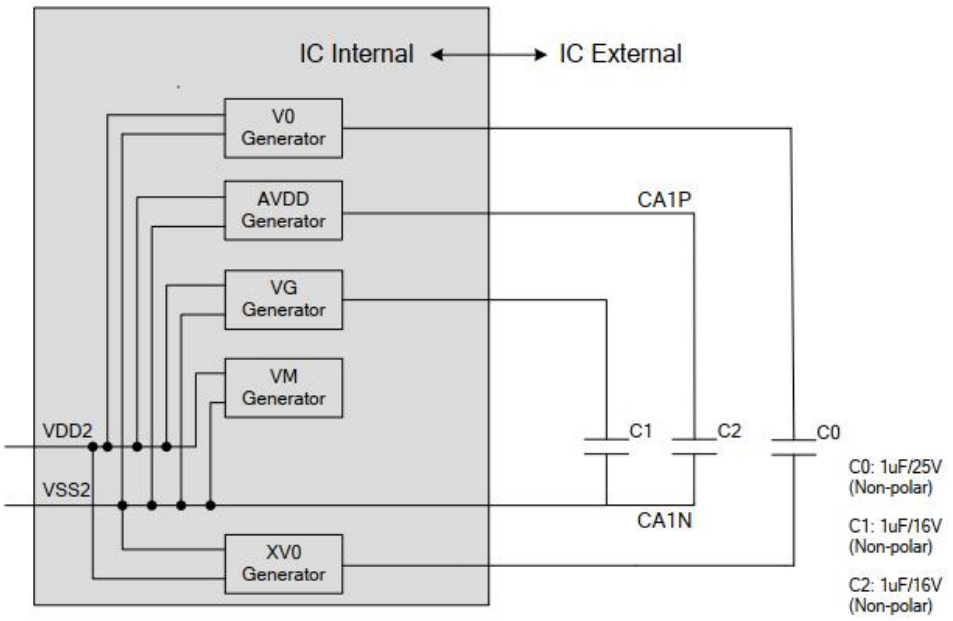


Figure 35 Internal Power Supply Circuit

Note:

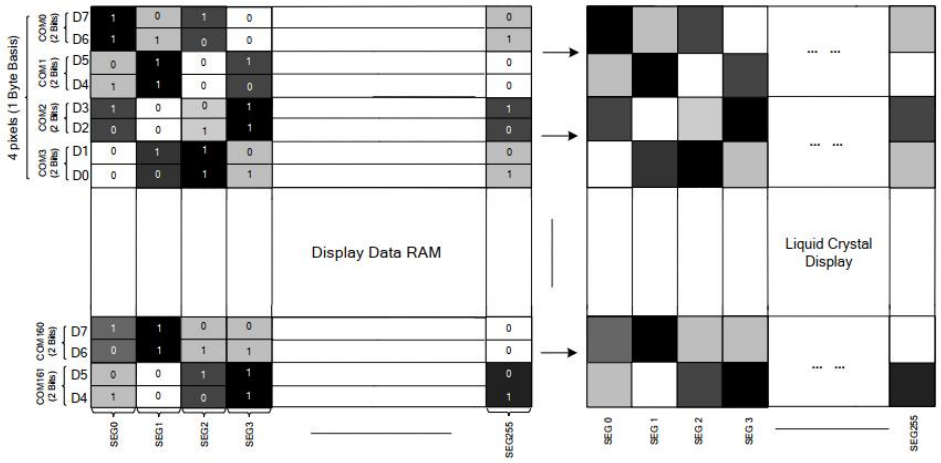
1. C0: 1uF/25V~2.2uF/25V (Default 1uF/25V)
2. C1: 1uF/16V~2.2uF/16V (Default 1uF/16V)
3. C2: 1uF/16V~2.2uF/16V (Default 1uF/16V)

4.3 Resetting the LCD module

Setting RSTB pin to —LII can initialize internal function. While RSTB is —LII, no instruction can be accepted.RSTB pin must connect to the reset pin of MPU and initialization by RSTB pin is essential before operating.After power-on, RAM data are undefined and the display status is —Display OFFII. It's better to initialize whole DDRAM (ex: fill all 00h or write a display pattern) before turning the Display ON.

The default values of registers are listed below:

4.4 Display Memory Map



2 Bits Data N=0~3		DDRAM		LCD
D2N+1	D2N			
1	1	1	1	
0	0	0	0	
1	0	1	0	
0	1	0	1	

Figure 21 DDRAM Mapping (4-Level Gray Scale Mode)

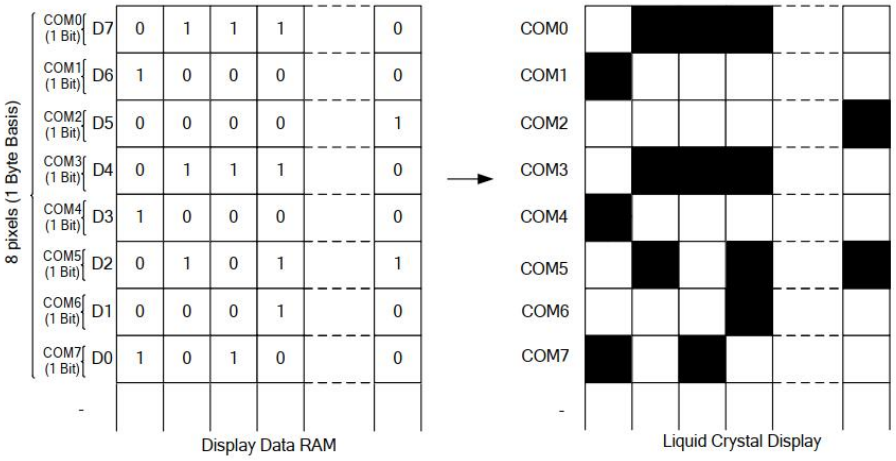


Figure 22 DDRAM Mapping (Monochrome Mode)

4.5 Display Commands

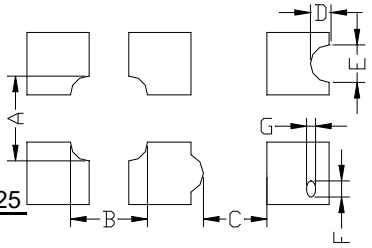
INSTRUCTION	A0	R/W	COMMAND BYTE								DESCRIPTION
			D7	D6	D5	D4	D3	D2	D1	D0	
1.Extension Command	0	0	0	0	1	1	EXT1	0	0	EXT0	Set extension instruction
Ext[1:0]=0,0 (Extension Command 1)											
2.Display ON/OFF	0	0	1	0	1	0	1	1	1	DSP	Set LCD display DSP=0: Display off DSP=1: Display on
3.Inverse Display	0	0	1	0	1	0	0	1	1	INV	Set inverse display INV=0: Normal display INV=1: Inverse display
4.All Pixel ON/OFF	0	0	0	0	1	0	0	0	1	AP	Set all pixel on mode, only for monochrome display AP=0: All pixel off mode AP=1: All pixel on mode
5.Display Control	0	0	1	1	0	0	1	0	1	0	Set display control CLD :Set CL dividing ratio DT[7:0] : Set the number of duty LF[4:0] : Set N-line inversion counter FI : Set the inversion type of frame at the end of common scan cycle
	1	0	0	0	0	0	0	CLD	0	0	
	1	0	DT7	DT6	DT5	DT4	DT3	DT2	DT1	DT0	
	1	0	0	0	LF4	FI	LF3	LF2	LF1	LF0	
6.Power Save	0	0	1	0	0	1	0	1	0	SLP	Set power save mode SLP=0: Sleep out mode SLP=1: Sleep in mode
7.Set Page Address	0	0	0	1	1	1	0	1	0	1	Set page address Starting page address: 00h≦YS≦28h Ending page address: YS≦YE≦28h
	1	0	YS7	YS6	YS5	YS4	YS3	YS2	YS1	YS0	
	1	0	YE7	YE6	YE5	YE4	YE3	YE2	YE1	YE0	
8.Set Column Address	0	0	0	0	0	1	0	1	0	1	Set column address Starting column address: 00h≦XS≦FFh Ending column address: XS≦XE≦FFh
	1	0	XS7	XS6	XS5	XS4	XS3	XS2	XS1	XS0	
	1	0	XE7	XE6	XE5	XE4	XE3	XE2	XE1	XE0	
9.Data Scan Direction	0	0	1	0	1	1	1	1	0	0	Set normal/ inverse display of address and address scan direction
	1	0	0	0	0	0	0	MV	MX	MY	
10.Write Data	0	0	0	1	0	1	1	1	0	0	Write data to DDRAM
	1	0	D7	D6	D5	D4	D3	D2	D1	D0	
11.Read Data	0	0	0	1	0	1	1	1	0	1	Read data from DDRAM (Only for parallel interface and I²C)
	1	1	D7	D6	D5	D4	D3	D2	D1	D0	
12.Partial In	0	0	1	0	1	0	1	0	0	0	Set partial area Starting partial display address: 00h≦PTS≦A1h Ending partial display address:
	1	0	PTS7	PTS6	PTS5	PTS4	PTS3	PTS2	PTS1	PTS0	

Note:

***a. For the details of the Display Commands, please refer to ST75256 data sheet**

n-Line reversal drive reset	0	0	1	1	1	0	0	1	0	0	Reset the line reversal drive
Built-in oscillator ON	0	0	1	0	1	0	1	0	1	1	Start the built-in oscillator circuit
External capacitor discharge	0	0	0	1	1	1	0	DISC			DISC = 000 (enable) DISC = 111 (disable)
NOP	0	0	1	1	1	0	0	0	1	1	Non-Operation command
Test	0	0	1	1	1	1	×	×	×	×	Don't use this instruction
Set OTP program	0	0	1	0	0	1	0	0	0	0	Set OTP program mode
OTP program control	0	0	OTPADJ	OTPPON	x	x	x	x	x	x	OTP control option OTPADJ = 1:OTP use OTPADJ = 0:OTP ignore OTPPON =1:OTP program enable OTPPON = 0:OTP program disable
Set contrast offset (1)	0	0	1	0	0	1	0	0	0	1	Set contrast offset mode (1)
	0	0	×	×	CTA5	CTA4	CTA3	CTA2	CTA1	CTA0	Set contrast offset register (1)
Set contrast offset (2)	0	0	1	0	0	1	0	0	1	0	Set contrast offset mode (2)
	0	0	×	×	×	CTB4	CTB3	CTB2	CTB1	CTB0	Set contrast offset register (2)
Set contrast offset (3)	0	0	1	0	0	1	0	0	1	1	Set contrast offset mode (3)
	0	0	×	×	×	CTC4	CTC3	CTC2	CTC1	CTC0	Set contrast offset register (3)
Read contrast offset(1)	0	0	1	0	0	0	1	1	0	0	Set contrast offset read mode (1)
	0	1	x	x	CTA5	CTA4	CTA3	CTA2	CTA1	CTA0	Read contrast offset(1)
Read contrast offset(2)	0	0	1	0	0	0	1	1	0	1	Set contrast offset read mode (2)
	0	1	x	x	x	CTB4	CTB3	CTB2	CTB1	CTB0	Read contrast offset(2)
Read contrast offset(3)	0	0	1	0	0	0	1	1	1	0	Set contrast offset read mode (3)
	0	1	x	x	x	CTC4	CTC3	CTC2	CTC1	CTC0	Read contrast offset(3)

5. Inspection Standards

Item	Criterion for defects	Defect type
1) Display on inspection	(1) Non display (2) Vertical line is deficient (3) Horizontal line is deficient (4) Cross line is deficient	Major
2) Black / White spot	Size Φ(mm) Acceptable number Φ≤0.3 Ignore (note) 0.3<Φ≤0.45 3 0.45<Φ≤0.6 1 0.6<Φ 0	Minor
3) Black / White line	Length (mm) Width (mm) Acceptable number L≤10 W≤0.03 Ignore 5.0≤L≤10 0.03<W≤0.04 3 5.0≤L≤10 0.04<W≤0.05 2 1.0≤L≤10 0.05<W≤0.06 2 1.0≤L≤10 0.06<W≤0.08 1 L≤10 0.08<W follows 2) point defect Defects separate with each other at an interval of more than 20mm	Minor
4) Display pattern	 $\frac{A+B}{2}\leq 0.28$ | 0<C | $\frac{D+E}{2}\leq 0.25$ | $\frac{F+G}{2}\leq 0.25$ Note: 1) Up to 3 damages acceptable 2) Not allowed if there are two or more pinholes every three-fourth inch.	Minor
5) Spot-like contrast irregularity	Size Φ(mm) Acceptable Number Φ≤0.7 Ignore (note) 0.7<Φ≤1.0 3 1.0<Φ≤1.5 1 1.5<Φ 0 Note: 1) Conformed to limit samples. 2) Intervals of defects are more than 30mm.	Minor
6) Bubbles in polarizer	Size Φ(mm) Acceptable Number Φ≤0.4 Ignore (note) 0.4<Φ≤0.65 2 0.65<Φ≤1.2 1 1.2<Φ 0	Minor
7) Scratches and dent on the polarizer	Scratches and dent on the polarizer shall be in the accordance with “2) Black/white spot”, and “3) Black/White line”.	Minor
8) Stains on the surface of LCD panel	Stains which cannot be removed even when wiped lightly with a soft cloth or similar cleaning.	Minor
9) Rainbow color	No rainbow color is allowed in the optimum contrast on state within the active area.	Minor
10) Viewing area encroachment	Polarizer edge or line is visible in the opening viewing area due to polarizer shortness or sealing line.	Minor
11) Bezel appearance	Rust and deep damages that are visible in the bezel are rejected.	Minor
12) Defect of land surface contact	Evident crevices that are visible are rejected.	Minor
13) Parts mounting	(1) Failure to mount parts (2) Parts not in the specifications are mounted (3) For example: Polarity is reversed, HSC or TCP falls off.	Minor
14) Part alignment	(1) LSI, IC lead width is more than 50% beyond pad outline. (2) More than 50% of LSI, IC leads is off the pad outline.	Minor
15) Conductive foreign matter (solder ball, solder hips)	(1) 0.45<Φ, N≥1 (2) 0.3<Φ≤0.45, N≥1, Φ: Average diameter of solder ball (unit: mm) (3) 0.5<L, N≥1, L: Average length of solder chip (unit: mm)	Minor
16) Bezel flaw	Bezel claw missing or not bent	Minor
17) Indication on name plate (sampling indication label)	(1) Failure to stamp or label error, or not legible.(all acceptable if legible) (2) The separation is more than 1/3 for indication discoloration, in which the characters can be checked.	Minor

6. Handling Precautions

6.1 Mounting method

A panel of LCD module made by our company consists of two thin glass plates with polarizers that easily get damaged.

And since the module in so constructed as to be fixed by utilizing fitting holes in the printed circuit board (PCB), extreme care should be used when handling the LCD modules.

6.2 Cautions of LCD handling and cleaning

When cleaning the display surface, use soft cloth with solvent (recommended below) and wipe lightly.

-Isopropyl alcohol

-Ethyl alcohol

-Trichlorotriflorothane

Do not wipe the display surface with dry or hard materials that will damage the polarizer surface.

Do not use the following solvent:

-Water

-Ketene

-Aromatics

6.3 Caution against static charge

The LCD module use C-MOS LSI drivers. So we recommend you:

Connect any unused input terminal to V_{dd} or V_{ss}. Do not input any signals before power is turned on, and ground your body, work/assembly areas, assembly equipment to protect against static electricity.

6.4 Packaging

-Module employs LCD elements, and must be treated as such. Avoid intense shock and falls from a height.

-To prevent modules from degradation, do not operate or store them exposed direct to sunshine or high temperature/humidity.

6.5 Caution for operation

-It is an indispensable condition to drive LCD module within the limits of the specified voltage since the higher voltage over the limits may cause the shorter life of LCD module.

-An electrochemical reaction due to DC (direct current) causes LCD undesirable deterioration so that the uses of DC (direct current) drive should be avoided.

-Response time will be extremely delayed at lower temperature than the operating temperature range and on the other hand at higher temperature LCD module may show dark color in them. However those phenomena do not mean malfunction or out of order of LCD module, which will come back in the specified operating temperature.

6.6 Storage

In the case of storing for a long period of time, the following ways are recommended:

-Storage in polyethylene bag with the opening sealed so as not to enter fresh air outside in it. And with not desiccant.

-Placing in a dark place where neither exposure to direct sunlight nor light is. Keeping the storage temperature range.

-Storing with no touch on polarizer surface by any thing else.

6.7 Safety

-It is recommendable to crash damaged or unnecessary LCD into pieces and to wash off liquid crystal by either of solvents such as acetone and ethanol, which should be burned up later.

-When any liquid leaked out of a damaged glass cell comes in contact with your hands, please wash it off well at once with soap and water.